Step by Step Design Tutorial of a fixed-frequency adapter < 75 W with very low power consumption

Presented by: Petr Papica
Agenda

• Application and requirements
• Flyback converter basics
• Flyback converter parasitic
• Design step 1: Power stage
• Design step 2: Efficiency optimization
• Design step 3: Control mode and protections
• Design step 4: No Load Input Power
• Design step 5: Magnetics
• Design step 6: EMI
• Demoboard example
The flyback, a popular structure

- The flyback converter is widely used in consumer products
- Ease of design, low-cost, well-known structure
  - Poor EMI signature, bulky transformer, practical up to 150 W

![DVD player](flyback) ≈ 10 – 35 W

![charger](flyback) ≈ 3 – 5 W

![notebook](flyback) ≈ 40 – 180 W
EPA 2.0 (External Power Supplies)

EPA ENERGY STAR Version 2.0 EPS Voluntary Specification
(Effective November 1, 2008)

Energy-Efficiency Criteria for Ac-Ac and Ac-Dc External Power Supplies
in Active Mode: Standard Models

<table>
<thead>
<tr>
<th>Nameplate Output Power ($P_{no}$)</th>
<th>Minimum Average Efficiency in Active Mode (expressed as a decimal)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 to ≤ 1 watt</td>
<td>$\geq 0.480 \times P_{no} + 0.140$</td>
</tr>
<tr>
<td>&gt; 1 to ≤ 49 watts</td>
<td>$\geq [0.0626 \times \ln(P_{no})] + 0.622$</td>
</tr>
<tr>
<td>&gt; 49 watts</td>
<td>$\geq 0.870$</td>
</tr>
</tbody>
</table>

*(was > 0.84 in previous version 1.1)*

Energy Consumption Criteria for No-Load

<table>
<thead>
<tr>
<th>Nameplate Output Power ($P_{no}$)</th>
<th>Maximum Power in No-Load</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>AC-AC EPS</td>
</tr>
<tr>
<td>0 to &lt; 50 watts</td>
<td>≤ 0.5 watts</td>
</tr>
<tr>
<td>≥ 50 to ≤ 250 watts</td>
<td>≤ 0.5 watts</td>
</tr>
</tbody>
</table>

*(< 0.5 W in 1.1)*

*(< 0.75 W in 1.1)*
EPS 5.0 (ENERGY STAR® Program Requirements for Computers)

- Defines $E_{TEC}$ for different types of products as a Typical Energy Consumption
- For the desktop and notebook product categories $E_{TEC}$ will be determined by the following formula:

$$E_{TEC} = \frac{8760}{1000} \times (P_{off} \times T_{off} + P_{sleep} \times T_{sleep} + P_{idle} \times T_{idle})$$

- where all $P_x$ are power values in watts, all $T_x$ are Time values in % of year, and the TEC $E_{TEC}$ is in units of kWh and represents annual energy consumption based on mode weightings

- The light load efficiency and no load consumption is more important

$E_{TEC}$ requirement desktops and notebooks

<table>
<thead>
<tr>
<th>TEC (kWh)</th>
<th>Desktops and Integrated Computers (kWh)</th>
<th>Notebook Computers (kWh)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Category A: ≤ 148.0</td>
<td>Category A: ≤ 40.0</td>
</tr>
<tr>
<td></td>
<td>Category B: ≤ 175.0</td>
<td>Category B: ≤ 53.0</td>
</tr>
<tr>
<td></td>
<td>Category C: ≤ 209.0</td>
<td>Category C: ≤ 88.5</td>
</tr>
<tr>
<td></td>
<td>Category D: ≤ 234.0</td>
<td></td>
</tr>
</tbody>
</table>

- Effective from July 1, 2009 (except: game consoles from July 1, 2010)
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An isolated buck-boost

- The flyback converter is an isolated version of the buck-boost cell
- By rotating the switch, we obtain a ground-referenced isolated converter
- Keep this in mind for the small-signal analysis!
On-time and freewheel

\[ V(\text{SW} / \text{D}) = \text{Vin} \]

\[ V(\text{SW} / \text{D}) = \text{Vout} \]

Circulates in the same direction

\[ I_{\text{peak}} = I_{\text{valley}} + \frac{V_{\text{in}}}{L} t_{\text{on}} \]

\[ I_{\text{valley}} = I_{\text{peak}} - \frac{V_{\text{out}}}{L} t_{\text{off}} \]

SW is closed, D is blocked

SW is open, D is closed

- When the switch closes, current ramps-up in \( L \)
- At the switch opening, the stored energy is dumped into \( C \)
The flyback circuit

- Similar buck-boost equations hold when scaled by the turn ratio $N$
- The switch is now ground referenced for an easier drive
- We have galvanic isolation between the primary and the secondary
The turn-on event

The controller instructs the power switch to turn on.

The current increases in the inductor in relationship to \( V_{in} \) and \( L_p \).

The output capacitor supplies the load on its own.

Simplified, no leakage.
Applying volt-second balance, CCM

\[ V_{Lp}(t) = V_{in} + \frac{V_{out}}{N} \]

\[ t_{on} = DT_{sw} \quad t_{off} = (1-D)T_{sw} \]

Reflected voltage

\[ V_{DS,off} = V_{in} + \frac{V_{out}}{N} = V_{in} + V_r \]

dc transfer function in CCM

\[ \frac{V_{out}}{V_{in}} = \frac{Nt_{on}}{t_{off}} = \frac{NDT_{sw}}{(1-D)T_{sw}} = \frac{ND}{(1-D)} \]

Simplified, no leakage
Applying volt-second balance, DCM

\[ \frac{V_{out}}{V_{in}} = D \sqrt{\frac{R_{\text{load}}}{2L_p F_{sw}}} \]

dc transfer function in DCM

\[ N \text{ no longer plays a role} \]

\[ R_{\text{load}}, L_p \text{ and } F_{sw} \text{ do} \]
Flyback, typical waveforms

- A simple flyback circuit **without** parasitic elements
- It runs open-loop for the sake of simplicity
- Vout = 8 V
Flyback, typical waveforms, CCM

1. Input current $I_{in}(t)$
2. Diode blocks
3. Voltage waveforms $V_{DS}(t)$, $V_{out}(t)$
4. Output capacitor refueling
5. Load current $I_d(t)$
Flyback, typical waveforms, DCM

- Input current: $I_{in}(t)$
- Output current: $I_{Lp}(t)$
- Diode blocks
- $V_{out}/N + V_{in}$
- $E_{valley} = 0$
- $E_{peak}$
- $V_{DS}(t)$

$V_{DS}$ is back to $V_{in}$ when all SW are blocked.
Energy transfer in CCM and DCM

\[ E_{L_p,\text{valley}} = \frac{1}{2} L_p I_{\text{valley}}^2 \]  
Initially stored energy

\[ E_{L_p,\text{peak}} = \frac{1}{2} L_p I_{\text{peak}}^2 \]  
Stored energy at \( t_{\text{on}} \)

\[ E_{L_p,\text{accu}} = \frac{1}{2} L_p I_{\text{peak}}^2 - \frac{1}{2} L_p I_{\text{valley}}^2 = \frac{1}{2} L_p \left( I_{\text{peak}}^2 - I_{\text{valley}}^2 \right) \]  
Accumulated energy at \( T_{\text{sw}} \)

Power (watts) is energy (joules) averaged over time (a switching cycle, seconds)

\[ P_{\text{out}} = \frac{1}{2} \left( I_{\text{peak}}^2 - I_{\text{valley}}^2 \right) L_p F_{\text{sw}} \eta \]  
CCM

\[ P_{\text{out}} = \frac{1}{2} I_{\text{peak}}^2 L_p F_{\text{sw}} \eta \]  
DCM, \( I_{\text{valley}} = 0 \)

Eta, the efficiency
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The leakage inductance

- The coupling in a transformer is not perfect
- Some induction lines couple in the air: leakage flux
An equivalent transformer model

- For a two-winding transformer, the model is simple:
  - Two leakage inductors
  - One magnetizing inductor
The leakage role

The switch closes:
Current flows in $L_{\text{leak}}$ and $L_p$

The switch opens:
The current charges the lump capacitor
Drain-source excursion

\[ V_{DS,max} = V_{in} + \left( \frac{V_{out} + V_f}{N} \right) + I_{peak} \sqrt{\frac{L_{leak}}{C_{lump}}} \]

Reflected \( V_{out} \)

Characteristic impedance

Need to limit the excursion!
The need of a clamp

- The clamp is made by a low impedance voltage source
- When the drain reaches $V_{in} + V_{clamp}$, the clamp diode conducts
A reduced secondary-side current

\[ I_{Lp}(t) \quad I_{\text{peak}} = 236 \text{ mA} \quad I'_{\text{peak}} = 210 \text{ mA} \]

\[ \Delta t = 480 \text{ ns} \]

Leakage inductor reset sequence

\[ I_{\text{d,peak}} = 2.1 \text{ A} \]

\[ V_{DS}(t) \]

www.onsemi.com
Ringing and turn-on in the valleys?

\[ V_{in} + V_{clamp} \]

\[ V_r + V_{in} \]

\[ e^{-\frac{R}{2L}} \]

\[ V_r \]

\[ t_v \]

\[ V_{DS}(t) \]

\[ t_v = \frac{1}{2f_0} = \pi \sqrt{(L_p + L_{leak})C_{lump}} \]

- Wait until the drain voltage is minimum and reduce turn-on losses: valley switching!
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Power stage: Schematic of flyback converter

\[ N = \frac{N_{\text{sec}}}{N_{\text{prim}}} \]
Power stage design: Bulk capacitor

- Output power $P_{out}$
  
  $$P_{out} = V_{out} \cdot I_{out}$$

- Estimation of input power $P_{in}$
  
  $$P_{in} = \frac{P_{out}}{\eta}$$  
  Estimate the $\eta$ based on the EPA standard

- Average input current $I_{in,avg}$
  
  $$I_{in,avg} = \frac{P_{in}}{V_{bulk, min}}$$

- Design the bulk capacitor for the maximum output power and the minimum input line voltage.
Power stage design: Bulk capacitor

- **1st current approach**

\[
C_{bulk} = \frac{1}{2} f_{line} \cdot \frac{I_{in,avg}}{\Delta V_{bulk}} \left[ 1 - \frac{1}{\pi} \cos^{-1} \left( 1 - \frac{\Delta V_{bulk}}{V_{peak}} \right) \right]
\]

Simple current approach:

\[
C_{bulk} = \frac{I_{in,avg} \cdot t_2}{\Delta V_{bulk}}
\]

Use \(t_2=7.5\) to 8.5ms for \(f_{line}=50\text{Hz}\)

- **2nd power approach**

\[
C_{bulk} = \frac{2 \cdot P_{in} \cdot t_2}{V_{peak}^2 - V_{min}^2}
\]

**Consideration:**

Low volume bulk: large ripple, better PF, lower input RMS current

High volume bulk: low ripple, bad PF, high input RMS current
Power stage design: Drain voltage

- $V_{ds}(t)$
- $V_{ds_{max}}$
- $V_{ds_{pk}}$
- $V_{leak}$
- $V_{clamp}$
- $V_{r}$
- $V_{bulk}$
- $t_{on}$
- $t_{off}$
- $T_{sw}$
- $t_{rec}$
- $t_{leak}$
Power stage design: Transformer ratio

Transformer ratio – consideration of the $V_{DSS}$ of used Q1

$$N = \frac{k_C \cdot (V_{out} + V_{f,diode})}{0.85 \cdot V_{DS,\text{max}} - 20V - V_{\text{bulk,max}}}$$

$$k_C = \frac{V_{\text{clamp}}}{V_r}$$

The 20V means margin for clamping diode turning-on overshoot.

Reflected voltage $V_r$ at primary from secondary

$$V_r = \frac{V_{out} + V_{f,diode}}{N}$$

Maximum duty cycle $DC_{\text{max}}$

In CCM operation:

$$DC_{\text{max}} = \frac{V_r}{V_r + V_{\text{bulk,min}}}$$

In DCM operation doesn’t depend on N:

$$DC_{\text{max}} = \frac{V_{out}}{V_{\text{bulk,min}}} \cdot \sqrt{\frac{2 \cdot L_{\text{prim}} \cdot F_{sw}}{R_{\text{load, min}}}}$$
Power stage design: Current ripple

The average shared transformer current reflected to primary winding $I_{L,\text{avg}}$

$$I_{L,\text{avg}} = \frac{I_{in,\text{avg}}}{DC_{\text{max}}}$$

Choose the relative ripple $\delta_{I_r}$: it affects the operation in the CCM or DCM

- For universal AC input design use the $\delta_{I_r}$ in range 0.5 to 1.0
- For European AC input use the $\delta_{I_r}$ in range 0.8 to 1.6

$$\Delta I = \delta_{I_r} \cdot I_{L,\text{avg}}$$

$$I_{\text{peak}} = I_{L,\text{avg}} \cdot \left(1 + \frac{\delta_{I_r}}{2}\right)$$

$$I_{\text{valley}} = I_{L,\text{avg}} \cdot \left(1 - \frac{\delta_{I_r}}{2}\right)$$
Power stage design: Primary inductance

Transformer primary winding inductance $L_{\text{prim}}$

$$L_{\text{prim}} = \frac{V_{\text{bulk, min}} \cdot DC_{\text{max}}}{F_{\text{sw}} \cdot \Delta I}$$

Maximum RMS value of the current flowing through primary winding $I_{\text{prim,RMS}}$

$$I_{\text{prim,RMS}} = \sqrt{DC_{\text{max}} \cdot \left( I_{\text{peak}}^2 - I_{\text{peak}} \cdot \Delta I + \frac{\Delta I^2}{3} \right)}$$

Maximum RMS value of the current flowing through secondary winding $I_{\text{sec,RMS}}$

$$I_{\text{sec,peak}} = \frac{I_{\text{peak}}}{N} \quad \Delta I_{\text{sec}} = \frac{\Delta I}{N}$$

$$I_{\text{sec RMS}} = \sqrt{(1 - DC_{\text{max}}) \cdot \left( I_{\text{sec,peak}}^2 - I_{\text{sec,peak}} \cdot \Delta I_{\text{sec}} + \frac{\Delta I_{\text{sec}}^2}{3} \right)}$$
Power stage design: Q1 selection

Conduction loss at Q1 should be approx. 1% of the Pout

\[ R_{DSon} \leq \frac{P_{out}}{100 \cdot I_{prim,RMS}^2} \]

Then the right device is chosen by parameters \( V_{DSmax}, I_{peak}, t_{on}, t_{off} \)

Current sensing resistor \( R_{sense} \) selection

\[ R_{sense} = \frac{V_{ILIM}}{1.1 \cdot I_{peak}} \]
\[ P_{sense} = I_{prim,RMS}^2 \cdot R_{sense} \]

The 1.1 factor means 10% margin for \( L_{prim} \) and other parameters spread, to be able to deliver maximum power.
Power stage design: Secondary rectification

D1 selection:
Reverse voltage across D1

\[ PIV = V_{bulk,\text{max}} \cdot N + V_{out} \]

The next important parameters for D1 selection are \( I_{\text{sec,peak}} \), \( I_{out} \) and the fast and soft recovery

Cout selection:
Minimum \( C_{out} \) value

\[ C_{out} \geq \frac{I_{out} \cdot DC_{\text{max}}}{V_{out,\text{ripple}} \cdot F_{sw}} \]

The maximum allowed ESR of \( C_{out} \)

\[ ESR \leq \frac{V_{out,\text{ripple}}}{I_{\text{sec,peak}}} \quad \text{Dominant part} \]

\[ I_{Cout,\text{rms}} = \sqrt{I_{\text{sec,\text{rms}}}^2 - I_{out}^2} \]

It is recommended to use more parallel \( C_{out} \) for lowering the output voltage ripple.
Power stage design: Clamping network

TVS – losses in the suppressor: better at no load conditions

\[ P_{\text{clamp}} = E_{\text{clamp}} \cdot F_{\text{sw}} = \frac{1}{2} \cdot L_{\text{leak}} \cdot I_{\text{peak}}^2 \cdot F_{\text{sw}} \cdot \frac{V_{\text{clamp}}}{V_{\text{clamp}} - V_r} \]

RCD clamp – 1\textsuperscript{st} iteration: better EMI response

\[ R_{\text{clamp}} = \frac{2 \cdot V_{\text{leak}} \cdot V_{\text{clamp}}}{L_{\text{leak}} \cdot I_{\text{peak}}^2 \cdot F_{\text{sw}}} \]

\[ P_{\text{clamp}} = \frac{V_{\text{clamp}}^2}{R_{\text{clamp}}} \]

\[ C_{\text{clamp}} > \frac{V_{\text{clamp}}}{V_{\text{ripple}} \cdot R_{\text{clamp}} \cdot F_{\text{sw}}} \]

These values need to be optimized for the no load consumption and losses in slow clamping diode D2.
TVS vs RCD clamp comparison

Drain voltage ringing with TVS as clamp

Drain voltage ringing with RCD as clamp

Different $R_{damp}$ used in clamp

Ch1 – Drain, Ch3 – Clamp node
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Application schematic
The losses distribution measured without EMI filters and surge protecting NTC

<table>
<thead>
<tr>
<th>Component</th>
<th>Power loss [W]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input rectifier</td>
<td>1.52</td>
</tr>
<tr>
<td>Transformer</td>
<td>2.44</td>
</tr>
<tr>
<td>Primary switch</td>
<td>2.53</td>
</tr>
<tr>
<td>Secondary rectifier</td>
<td>2.78</td>
</tr>
</tbody>
</table>

Input line: 110 V / 60 Hz
Input power: 72.5 W
Output power: 63.62 W
Total loss power: 8.88 W
Efficiency: 87.75%
Optimization of efficiency

• There was not found excessive contributor of losses in the power stage of the flyback converter
• Losses in all components should be decreased
• Optimization approach:

  1) decreasing the losses in power stage by selection of primary switch Q1 and secondary rectifier D1
  2) decreasing the losses in power stage by decreasing losses in transformer
  3) try to improve the bridge rectifier (not much space)
  4) decreasing the conductive losses in EMI filters
  5) Do we need surge protecting NTC in case of “low value” bulk capacitor?
Influence of EMI filters

- Input EMI filter contributes to the conductive losses mainly at full load and low line condition
- The high inductance 22mH or more is needed to reject the “low” frequency emissions (below 1 MHz)
- There is needed to use two chamber CM choke or 2 CM mode chokes to reject the high frequency emissions above 10MHz
- Output EMI filter (CM choke) reject the high frequency emissions from the DC cord, only low inductance is needed → low Rdc → low conduction losses
- The most important are losses in the high inductance input common choke from the efficiency optimization point of view

Note from experiments:

There was found an influence of HF ripple at input current to the precision of measurement of input power using wattmeter YOKOGAWA WT210. There were measured lower input power with the connected 100uH common choke in comparison without any EMC filter. (at the same conditions) It is better always to use some EMI filter, with small Rdc to reject the error given by the noisy HF currents.
Transformer optimization result

The optimum ratio is given by the Q1 maximum break down voltage with 15% derating factor.

Decreasing the Ns/Np decreases the secondary winding losses and primary RMS current.

Decreasing the Ns/Np increases the Q1 switching losses and secondary RMS current.

The graph shows the relationship between transformer ratio Ns/Np and efficiency. The optimum ratio is indicated by the Q1 breakdown area. Decreasing the Ns/Np decreases the secondary winding losses and primary RMS current. Decreasing the Ns/Np increases the Q1 switching losses and secondary RMS current.
Improving Efficiency

• Sources of loss:

  – Switching losses:
    \[ P_{\text{loss(switching)}} = \frac{1}{2} \cdot C_{\text{DRAIN}} \cdot V_{\text{DRAIN (turn-off)}}^2 \cdot F_{\text{SW}} \]

  – Losses caused by leakage inductance:
    \[ P_{\text{loss(leak)}} = \frac{1}{2} \cdot L_{\text{leak}} \cdot I_{\text{peak}}^2 \cdot F_{\text{SW}} \]

• Ways to improve efficiency:

  – Lower the switching frequency \( F_{\text{SW}} \) ➡️ frequency foldback at light loads

  – Lower the Drain voltage at turn-off ➡️ valley switching
Synchronous rectification

- New SR controller NCP4303 coming in 2010
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Application schematic
The voltage-mode PWM generation

- In voltage-mode, one compares the error voltage to a fixed ramp.
- This is « Pulse Width Modulation » also called « PWM ».
The voltage-mode PWM generation

- The inductor current is sensed for safety only
The current-mode PWM generation

- In current-mode, the error voltage fixes the peak current
The current-mode PWM generation

- The sense resistor provides a **pulse-by-pulse** current limit
Same modulation between VM and CM

- Both modulators use trailing edge modulation

**Trailing** edge modulation

**Leading** edge modulation
NCP1237/38/87/88 flyback controller

**Value Proposition**

The NCP1237/38/87/88 series represents the next generation of fixed frequency PWM controllers. It targets applications where cost-effectiveness, reliability, design flexibility and low standby power are compulsory.

**Unique Features**

- High-voltage current source with built-in Brown-out and mains OVP
- Freq. reduction in light load conditions and skip mode
- Adjustable Over Power Protection

**Benefits**

- Fewer components and rugged design
- Extremely low no-load standby power
- Simple option to alter the max. peak current set point at high line

**Others Features**

- Latch-off input for severe fault conditions, allowing direct connection of NTC
- Timer-based protection: auto-recovery or latched
- Dual OCP option available
- Built-in ramp compensation
- Frequency jittering for a softened EMI signature
- Vcc operation up to 30 V

**Application Data**

<table>
<thead>
<tr>
<th></th>
<th>DSS</th>
<th>Dual OCP</th>
<th>Latch</th>
<th>Auto Recovery</th>
</tr>
</thead>
<tbody>
<tr>
<td>NCP1237A</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td>NCP1237B</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td>NCP1238A</td>
<td>Yes</td>
<td>No</td>
<td>Yes</td>
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<tr>
<td>NCP1238B</td>
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<td>No</td>
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<tr>
<td>NCP1287A</td>
<td>HV only</td>
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<tr>
<td>NCP1287B</td>
<td>HV only</td>
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<td>Yes</td>
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</table>

Various options available depending upon end applications needs

**Market & Applications**

- AC-DC adapters for notebooks, LCD monitor, game console, printers
- CE applications (DVD, STB)

**Ordering & Package Information**

- NCP1237/38xDR2G - NCP1287/88xDR2G
- SOIC-7 2500p per reel

www.onsemi.com
NCP1237/38/87/88 – Built-in Startup FET

A flyback auxiliary winding supplies biasing voltage in normal condition to save power.

High startup current to reduce charging time.

Low initial startup current to prevent damage if Vcc pin is shorted to ground.

No startup resistor!

Saves PCB area & saves power.
NCP1237/38/87/88 – Dynamic Self Supply (optional)

How it works...

Power ON → Current Source turns ON → $V_{cc}$ is rising; no output pulses
$V_{cc}$ reaches $V_{cc(on)}$ → Current Source turns OFF → $V_{cc}$ is falling; output is pulsing
$V_{cc}$ falls to $V_{cc(off)}$ → Current Source turns ON → $V_{cc}$ is rising; output is pulsing

Dynamic Self-Supply No need of auxiliary winding!
Startup current is low initially to prevent damage when $V_{CC}$ pin is grounded. Startup current is activated when $V_{CC}$ drops to $V_{CC(\text{off})}$. Hence, the voltage never drops below $V_{CC(\text{off})}$ after startup. Startup current is off when $V_{CC}$ reaches $V_{CC(\text{on})}$. 

Startup current level: 
- 8 mA
- 500 μA

Voltage levels:
- 0.6 V
- $V_{CC(\text{off})}$
- $V_{CC(\text{on})}$

www.onsemi.com
Detection independent of Ripple on HV pin  Can be connected to the half-wave rectified ac line
NCP1237/38/87/88 – Brown-out and Mains OVP

Timer-based detection [ ] Passes full line cycle drop-out
Current overshoot: do not underestimate it...

\[ I_{\text{peak, max}} = \frac{V_{\text{sense, max}}}{R_{\text{sense}}} + \frac{V_{\text{in, max}}}{L_p} t_{\text{prop}} \]

- Watch-out for clamp voltage variations, at start-up or in short-circuit
- The main problem comes from the propagation delay!
The compensation current creates an offset on the Current Sense signal.

Need to compensate for the effect of the propagation delay.

NCP1237/38/87/88 – Over Power Protection

Over Power Protection $\Rightarrow$ Maximum output power clamped
NCP1237/38/87/88 – Dual OCP threshold

Accommodates large output power transients

Suitable for printers

These protections use the Up/Down counters, like classical analog integration.
NCP1237/38/87/88 – 4 ms Soft Start

4 ms Soft Start  ➔ Stressless start-up phase

4 ms "digital" soft-start operation

Max. current setpoint envelope

without soft-start

with soft-start

voltage / current

V_{CC}

time

time
NCP1237/38/87/88 – Frequency Foldback

Switching frequency lowered at light load → Increased efficiency

Switching frequency clamped at 25 kHz → No audible noise
NCP1237/38/87/88 – Recover from Standby

Soft-Skip mode is left as soon as the voltage on the feedback pin reaches the TLD threshold.

Transient Load Detect Function (TLD) Improves Load Transient response time
An NTC thermistor can be directly connected to the IC

Less external components needed
CCM operation, current instabilities

Duty-cycle < 50%

Asymptotically stable

Duty-cycle > 50%

Asymptotically unstable
**CCM operation, curing current instabilities**

\[ \Delta I_L(nT_{sw}) = \Delta I_L(0) \left[ 1 - \frac{S_a}{S_2} \right] \]

\[ \frac{1 - \frac{S_a}{S_2}}{d + \frac{S_a}{S_2}} = \Delta I_L(0)(-a)^n \]

Must stay below 1

Up to \( d = 100\% \)

\[ \left| \frac{1 - \frac{S_a}{S_2}}{\frac{S_a}{S_2}} \right| < 1 \]

Inject ramp compensation

\[ S_a > 50\% S_2 \]
NCP1237/38/87/88 – Slope compensation

- There is a built-in slope compensation with no external setting.
- The internal slope compensation is activated if the duty cycle is higher than 40%.
- The amount of slope compensation is 5mV/% observed at CS pin.
Block schematic
Agenda

- Application and requirements
- Flyback converter basics
- Flyback converter parasitic
- Design step 1: Power stage
- Design step 2: Efficiency optimization
- Design step 3: Control mode and protections
  - Design step 4: No Load Input Power
- Design step 5: Magnetics
- Design step 6: EMI
- Demoboard example
Reducing No-load Input Power

• Static losses in the start-up circuit:
  – Start-up resistor permanently drawing current from the bulk capacitor

• Ways to lower the start-up circuit losses
  – With external start-up resistor ➔ Extremely low start-up current
  – Integrated start-up current source ➔ Extremely low leakage when off
  – Connect the start-up circuit to the half-wave rectified ac input

![Diagram showing NCP1351 and start-up resistors](image)
Reducing No-load Input Power

\[ R_{\text{startupHW}} = \frac{R_{\text{startup}}}{\pi} \]

Selected from bulk connection

\[ P_{R_{\text{startupHW}}} = \frac{P_{R_{\text{startup}}}}{4} \]

Brings a 21% reduction in power
No load input power reducing approach

- Decrease the transformer leakage inductance
- Use the controller IC with the frequency foldback and skip mode features
- Do not allow the DSS operation (Vcc cap increase)
- In case of low Vcc and high aux winding leakage increase the aux number of turns to disable the DSS
- Decrease the value of the Vcc damping resistor (may affect the EMI)
No load input power reducing approach

- Lower the M1 switching losses
- Optimize the clamping circuitry
- Reduce the losses in the secondary rectifier and its snubber
- Decrease the TL431 biasing
- Decrease the cross current through the feedback resistor divider
- Set a stable operation for all loading currents
- Do not use the output voltage indication LED
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Area product $A_p$

- There is defined the area product $A_p [m^4]$
- Product of effective window area $W_a [m^2]$ and iron cross section area $A_c [m^2]$

$$A_p = W_a \cdot A_c$$

- Allows fast, effective and optimal magnetic design
- Should be published in core datasheet
Window utilization factor $K_u$

$K_u$ is a measure of the amount of copper that appears in the window area of transformer. This window utilization factor is affected by:

1) Wire insulation
2) Wire lay (fill factor)
3) Bobbin area
4) Insulation required for multilayer windings or between windings

Typical values lay in range 0.35 to 0.48
The load coefficient $K_{\text{load}}$

- Flux density in magnetic should be designed at $I_{\text{peak}}$ with some margin (5%) to avoid saturation
- Do you really need 100% $I_{\text{out}}$ for 100% time??

If not, decrease core size!!

$$K_{\text{load}} = \frac{I_{\text{out,RMS}}}{I_{\text{out,RMS, max}}}$$

Example:
- Maximum DC output current is 3.5A, but it’s only needed for transients
- The long term RMS value is only 1.75A (at least 10 min.)
- Loading coefficient is only 0.5 (not 1) → core size is smaller
  → losses in core and in copper are smaller
Flyback transformer core sizing

The core size can be calculated by the $A_P$ factor in case of these inputs:

1. Converter parameters: $L_{\text{prim}}$, $I_{\text{peak}}$, $K_{\text{load}}$, $\delta I_r$, $DC_{\text{max}}$
2. Core maximum flux density $B_{\text{max}}$ considered with the hysteresis and eddy current losses at switching frequency $F_{\text{sw}}$
3. Winding parameters (utilization factors for primary and secondary windings $K_{u_{\text{prim}}}$, $K_{u_{\text{sec}}}$), (current densities in primary and secondary windings $J_{\text{prim}}$, $J_{\text{sec}}$)

$$A_P = \frac{L_{\text{prim}} \cdot I_{\text{peak}}^2}{B_{\text{max}}} \cdot K_{\text{load}} \cdot \left( \frac{\sqrt{DC_{\text{max}}}}{J_{\text{prim}} \cdot K_{u_{\text{prim}}}} + \frac{\sqrt{1 - DC_{\text{max}}}}{J_{\text{sec}} \cdot K_{u_{\text{sec}}}} \right) \cdot \sqrt{\frac{\delta I_r^2 + 12}{3 \cdot (\delta I_r + 2)^2}}$$

Now the appropriate core can be selected from the vendor products list by the $A_P$ factor.
Windings design

• Number of turns of primary winding

\[ NT_{\text{prim}} = \frac{L_{\text{prim}} \cdot I_{\text{peak}}}{B_{\text{max}} \cdot A_c} \]

• Number of turns of secondary winding

\[ NT_{\text{sec}} = N \cdot NT_{\text{prim}} \]

• Number of turns of auxiliary winding

\[ NT_{\text{aux}} = \frac{V_{CC} + V_{f,vcc}}{V_{out} + V_{f,diode}} \cdot NT_{\text{sec}} \]
Air gap length $l_g$

\[ l_g = \frac{N \cdot \mu_0 \cdot I_{\text{peak}}}{B_{\text{max}}} - \frac{\text{MPL}}{\mu_r} \]

in case of $l_g << \text{MPL}$

MPL – core magnetic path length

$\mu_0$ - permeability of vacuum

$\mu_r$ - permeability of core

In case an EE, RM or pot core is used, divide the calculated $l_g$ by factor 2, because your core has 2 air gaps in magnetic path
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How to improve EMI of my design?

- All switching loops with RF currents should have small area
- Divide input AC filter at two chokes to decrease the parasitic capacitance coupling
- CY – closes the current loop for the RF currents injected via transformer
Diode snubber design

- Snubber resistance value should be close to the characteristic impedance of ringing circuitry

$$R_{snubber} = \sqrt{\frac{L_{\text{leak,SEC}}}{C_d}}$$

$L_{\text{leak,SEC}}$ – the transformer leakage inductance observed from secondary side

$C_d$ – reverse direction diode capacitance

- RC time constant of the snubber should be small compared to the switching period but long compared to the voltage rise time

$$C_{snubber} \approx 3 \div 4 \cdot C_d$$
PCB Layout tips

- DRV loop
- Clamping loop
- Output loop
- Power switch loop
- Capacitor pads arrangement for better filtering RF currents
- Diode snubber
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Preliminary demonstration board

A typical 65 W notebook adapter (19 V output)

(optimizerized for EPS 2.0)
Schematic of preliminary demonstration board

A typical 65 W notebook adapter (19 V output)

(optimized for EPS 2.0)
Demonstration board Efficiency (measured with DC cord)

The DC cord length is 1.05m and copper cross sec. is 0.75mm²

<table>
<thead>
<tr>
<th>% of $P_{\text{OUT}_{\text{nom}}}$</th>
<th>$V_{\text{IN}}$</th>
<th>115 Vac/60Hz</th>
<th>230 Vac/60Hz</th>
</tr>
</thead>
<tbody>
<tr>
<td>100 % (65 W)</td>
<td>87.10 %</td>
<td>87.37 %</td>
<td></td>
</tr>
<tr>
<td>75 % (49 W)</td>
<td>87.52 %</td>
<td>87.63 %</td>
<td></td>
</tr>
<tr>
<td>50 % (32 W)</td>
<td>87.54 %</td>
<td>87.88 %</td>
<td></td>
</tr>
<tr>
<td>25 % (16 W)</td>
<td>87.79 %</td>
<td>85.96 %</td>
<td></td>
</tr>
</tbody>
</table>

Average at 115Vac is 87.32% and at 230 Vac is 87.21 %
# Demonstration board Standby Power

Light load and no load input power with the NCP1237

<table>
<thead>
<tr>
<th>$P_{OUT}$</th>
<th>$V_{IN}$</th>
<th>115 Vac/60Hz</th>
<th>230 Vac/50Hz</th>
</tr>
</thead>
<tbody>
<tr>
<td>10 %</td>
<td>86.55 %</td>
<td>83.74 %</td>
<td></td>
</tr>
<tr>
<td>(6.5 W)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5 %</td>
<td>85.40 %</td>
<td>78.72 %</td>
<td></td>
</tr>
<tr>
<td>(3.3 W)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 %</td>
<td>77.49 %</td>
<td>73.77 %</td>
<td></td>
</tr>
<tr>
<td>(0.65 W)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>No load</td>
<td>51.1 mW</td>
<td>73.5 mW</td>
<td></td>
</tr>
</tbody>
</table>
Demonstration board Efficiency

Efficiency [%]

Pout [W]

- 115 Vac - NCP1237
- 230 Vac - NCP1237

www.onsemi.com
Demonstration board conducted EMI

80% of full load (2.72A) at 230V/50Hz NCP1237B65kHz
NCP1237B100kHz frequency jittering

Ref1 – DRV frequency
NCP1237B100kHz frequency foldback

Ch1 – DRV, Ch2 – FB, Ref1 – DRV frequency
Load transient response from 20% to 100%

Ch1 – Drain, Ch2 – FB, Ch3 – Vout (AC coupling), Ch4 - Iout
Load transient response from 100% to 20%

Ch1 – Drain, Ch2 – FB, Ch3 – Vout (AC coupling), Ch4 - Iout
Conclusion

- Meeting the most recent requirements from ENERGY STAR® or IEC is possible with the classical **Flyback** converter.
- The new controller NCP1237/37/87/88 with frequency foldback and skip-mode at light load makes it possible.
- Average efficiencies above **87%** are possible.
- No-load input power below **300 mW** is possible.
- No-load input power below **100 mW** is achievable, although the controller alone cannot ensure this. The whole power supply must be designed to reduce power waste.
References

Tutorial and Application notes:

http://www.onsemi.com/pub_link/Collateral/TND376-D.PDF

http://www.onsemi.com/pub_link/Collateral/AND8461-D.PDF

http://www.onsemi.com/pub_link/Collateral/DN06074.PDF

Feedback loop design spreadsheet:

http://www.onsemi.com/pub/Collateral/FLYBACK DWS.XLS.ZIP
Thank You! Any Questions?
Backup
Over power compensation

The overpower compensation affects the primary peak current, by the following formula:

\[ I_{\text{PEAK}} = \frac{V_{\text{CS, int}}}{R_{\text{sense}}} + V_{\text{bulk}} \cdot \left( \frac{t_{\text{PROP}}}{L_p} - g_{\text{OPP}} \cdot \frac{R_{\text{OPP}}}{R_{\text{sense}}} \right) + V_{\text{off}} \cdot g_{\text{OPP}} \cdot \frac{R_{\text{OPP}}}{R_{\text{sense}}} \]

Then the overpower compensation resistor can be calculated:

\[ R_{\text{OPP}} = \frac{t_{\text{PROP}} \cdot R_{\text{sense}}}{L_p \cdot g_{\text{OPP}}} \]

The over power compensating resistor affects only the \( I_{\text{peak}} \) value, but in CCM the output power is given by the following formula, where \( I_{\text{valley}} \) plays a role:

\[ P_{\text{out}} = \frac{1}{2} \cdot \eta \cdot L_{\text{prim}} \cdot F_{\text{sw}} \cdot \left( I_{\text{peak}}^2 - I_{\text{valley}}^2 \right) \]
2nd level over current protection

The overpower compensation affects the 2nd level over current protection by the addition of bulk voltage feed forward.

\[ I_{TRAN} = \frac{V_{CStra}}{R_{sense}} - (V_{bulk} - V_{off}) \cdot g_{OPP} \cdot \frac{R_{OPP}}{R_{sense}} \]

The 2nd level over current protection can be used for reducing the transformer size to \( \frac{1}{2} \) and keeping the peak power capability.
Spread sheet design of OPC

OPC design spread sheet was created and the user can choose the right $R_{OPP}$ and it’s effect to $I_{peak}$, $I_{tran}$, $P_{out}$ and $P_{tran}$:

Inputs:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output voltage</td>
<td>Vout [V]</td>
</tr>
<tr>
<td>Primary turns</td>
<td>N1 [-]</td>
</tr>
<tr>
<td>Secondary turns</td>
<td>N2 [-]</td>
</tr>
<tr>
<td>Ramp Comp at CS</td>
<td>RaCo [mV/%]</td>
</tr>
<tr>
<td>Maximum int set point</td>
<td>V\text{ilimit} [V]</td>
</tr>
<tr>
<td>Sensing resistor</td>
<td>Rsense [Ohm]</td>
</tr>
<tr>
<td>Propagation delay</td>
<td>t\text{prop} [ns]</td>
</tr>
<tr>
<td>Primary inductance</td>
<td>Lp [uH]</td>
</tr>
<tr>
<td>Vin to lopp ratio</td>
<td>gopp [uS]</td>
</tr>
<tr>
<td>Over power comp resistor</td>
<td>Ropp [Ohm]</td>
</tr>
<tr>
<td>Switching frequency</td>
<td>Fsw [kHz]</td>
</tr>
<tr>
<td>2nd level overcurrent prot</td>
<td>Vc\text{stran} [V]</td>
</tr>
</tbody>
</table>
Spread sheet design of OPC

Keeping constant $I_{\text{peak}}$ in CCM mode tends to $I_{\text{valley}}$ decreasing with increasing the $V_{\text{in}}$. That’s why the maximum output deliverable power $P_{\text{out}}$ increases with increasing $V_{\text{in}}$. Choose the right compensation.