SECONDARY FREQUENCY STANDARD FOR EXPERIMENTAL SATELLITE

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Abstract: *This paper deals with the design of 5 MHz PLL oscillator that will serve as secondary frequency standard onboard of an experimental communication satellite. An attention was given to low phase noise of generated signal, robust design and low power consumption.*

Introduction

The experimental satellite AMSAT Phase 3E will carry communication equipment, which should be synchronized by onboard ultra-stable 5 MHz oscillator (USO). The USO holds excellent frequency accuracy as well as long term frequency stability and very low phase noise, respectively. However, essential requirement for USO is reliability. For this reason the USO needs a back up. Well performed free running VCXO that can be locked to USO by phase lock loop (if USO signal exists) has been selected as optimal arrangement for this purpose.

Design

The block diagram of the final arrangement is shown in Figure 1. Input signal from USO is formed by Schmitt trigger inverter. Next circuit detects the USO signal. If this signal is detected then the PLL is active and VCXO is synchronized by that signal. When the USO is out of order, then USO signal is not detected and a constant voltage for VCXO's tuning input is supplied by a mode detector. In this case the VCXO runs free at frequency of 5 MHz quartz.

As VCXO a Colpitts quartz oscillator is used. To obtain necessary realignment of output frequency serial inductors are placed between voltage variable capacitor and tuned quartz. By this way has been achieved 334 Hz/V conversion gain.

The satellite bus voltage is 14 V. All parts of PLL oscillator circuit are designed for voltage 5 V, except the buffer amplifier OPAMP that needs 8 V. The stabilizer for 8 V is linear. As 5 V power supply is applied DC-DC converter with IC LM2574. The efficiency of switched stabilizer is better than 40 % instead circa 20 % for the linear stabilizer under the same condition.

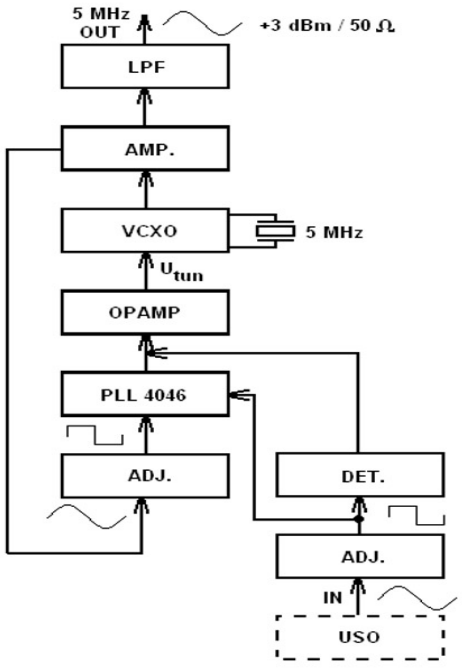

Fig. 1. Block diagram of the arrangement

Construction

The layout is designed as the both-side PCB on a substrate FR4. The circuit of frequency standard is soldered in a shielding box with dimensions 60 x 48 x 23 mm. Power supply is injected by a feed-through soldered capacitor. Connection to other outside circuits of this box - connectors IN and OUT - is done by the SMA connectors. Photos of 5 MHz secondary frequency standard are given in Figure 2.

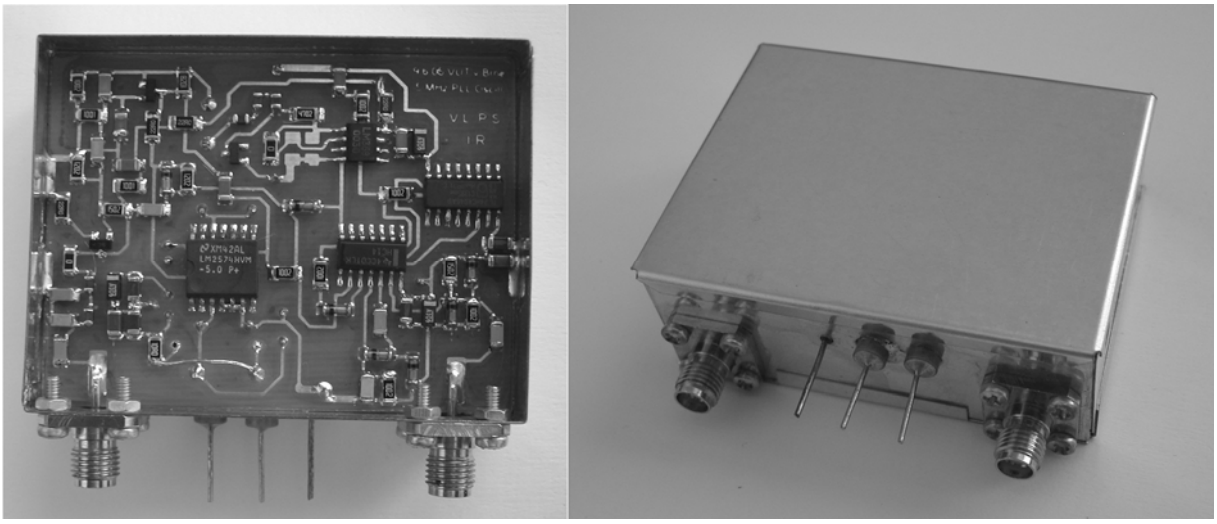

Fig. 2. Realized 5 MHz secondary frequency standard

Measurements

Parameters of described secondary frequency standard have been measured and achieved values are presented in the Table I. The measurement has been performed for both possible cases - for state with and without the USO signal.

Table I. Secondary frequency standard parameters

Without USO		I_{cc}	18.52	mA
		$f_{o\ open}$	5.000048	MHz
		$f_{o\ close}$	5.000070	MHz
		P_{out}	3.44	dBm
		PN	−104.5	dBc@100Hz
With USO	Lock	I_{cc}	19.90	mA
		f_{min}	4.999380	MHz
		f_{max}	5.001050	MHz
		PN	−103.1	dBc@100Hz
	Capture	f_{min}	4.999410	MHz
		f_{max}	5.001000	MHz
		$P_{in\ min}$	4.6	dBm

Value $f_{o\ open}$ in the Table I. is frequency for free running mode without sheet cover and value $f_{o\ close}$ is measured with sheet cover. The I_{cc} value is valid for supply voltage 14 V.

The phase noise of secondary frequency standard output signal in the free running state is given in Figure 3.

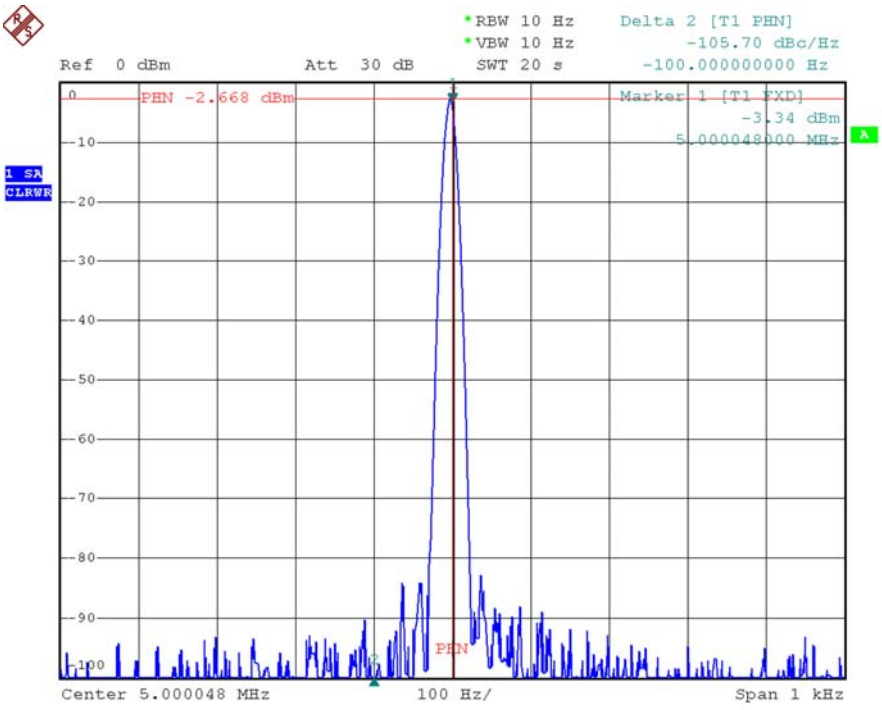

Fig. 3. Phase noise of the non synchronized output signal (free running state)

The phase noise course of secondary frequency standard output signal for lock state is given in Figure 4. The phase noise of reference oscillator signal used in this measurement is better than −106.2dBc@100Hz and reference signal level P_{ref} = −2,17 dBm.

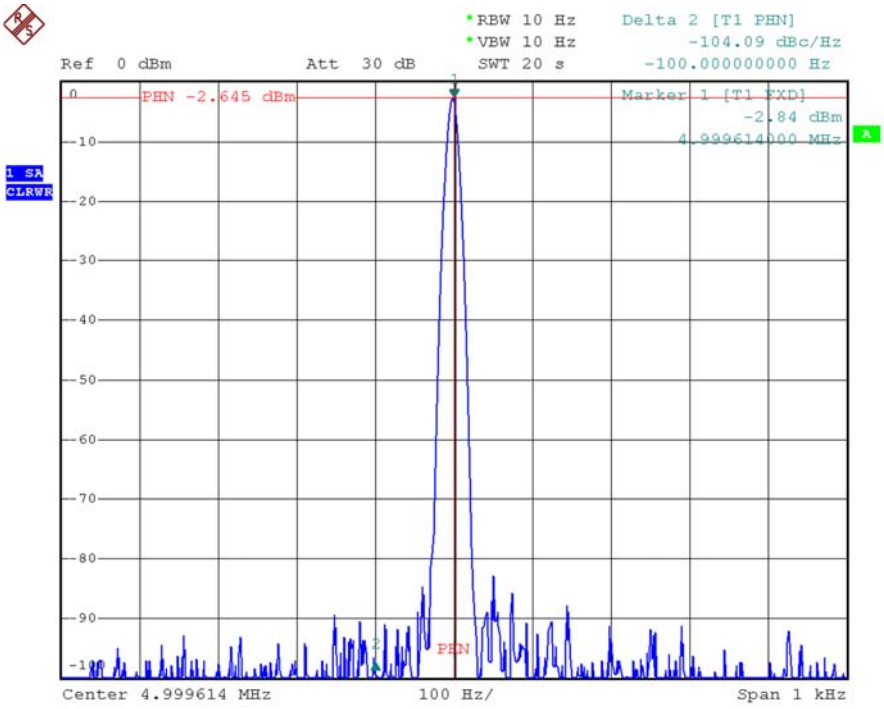

Fig. 4. Phase noise of secondary frequency standard output signal in phase lock state

The spectrum of oscillator output signal for PLL lock state up to 3th harmonic is given in Figure 5. Apparently, the second harmonic suppression is better than 25.8 dB.

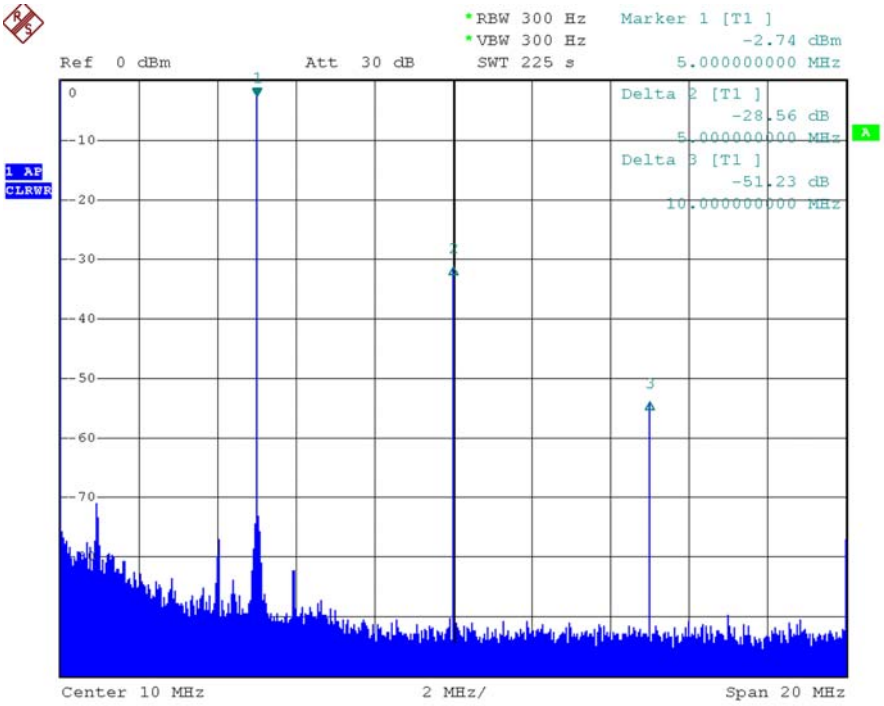

Fig. 5. Secondary frequency standard output signal spectrum in phase lock state

Conclusion

Described unit of the secondary frequency standard will be applied in several sections of the P3E satellite communication equipment. Achieved spectral purity promises appropriate high level applications like coherent ranging and slow rate data communication at reduced bandwidth. At present, the described secondary frequency standard is under pre-launch tests in laboratories in Finland and Belgium.

Acknowledgment

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References

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