Effective DSP Methods of PSK Feedback Timing Synchronization

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Abstract. *This paper deals with simplification and improvement of data timing synchronization algorithms. Timing error synchronizers are usually the most complicated subsystems in the demodulator, and limit the DSP technique used for the high-rate application. This article is focused on feedback timing estimators for PSK modulation schemes, and shows modifications of widely used algorithms, that are suitable for the DSP implementation, as well as reach better parameters of the detection process. The methods applied in the evaluation of a timing error detector, which is a crucial part of the synchronizer, are described in the last part.*

Keywords

Additive white Gaussian noise, delay lock loop, digital signal processing, early-late detector, ML criterion, Mueller-Mueller detector, normalized timing error variance, phase shift keying, timing synchronization, timing error detector, raised-cosine pulse shaping, zero-crossing detector.

1. Introduction

Structures of all feedback timing synchronizers result from a general closed loop, where the tracked parameter is the delay between optimum and actual symbol timings. The analytical description of such a closed loop corresponds to a phase lock loop (PLL) analysis, where the phase error is replaced by the time error or the delay. Consequently, the feedback timing synchronizer presents a delay lock loop (DLL) (Fig. 1).

Considering an I-Q demodulator, the timing estimation is more complicated than the phase estimation. The phase error determination is a simple procedure executed by the Phase Error Detector (PED). The phase can be easily extracted from the signal components (I and Q) for any sample:

$$\varphi = \arctan\frac{y_Q}{y_I}. \tag{1}$$

However, the delay (or symbol timing error) determination needs at least two consecutive samples. The system, which solves this operation, is called as Timing Error Detector (TED). Choice of a proper TED algorithm is a crucial point of timing synchronizer design. Above all, it depends on the modulation constellation, impulse shaping and the expected signal-to-noise ratio. The best results are reached by the application of maximum-likelihood (ML) criterion.

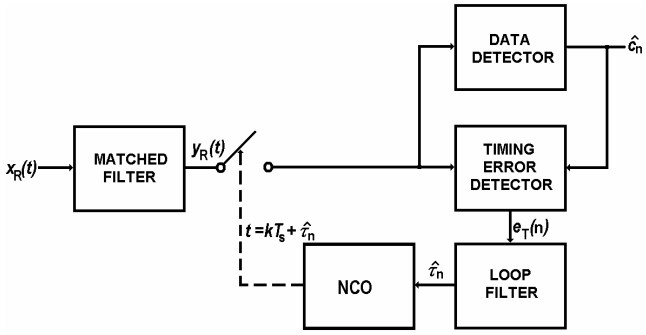

Fig. 1. Flow representation of the feedback timing synchronizer.

Mathematical operations for obtaining ML-based equations for TED are derived completely in literature [1]. There are three fundamental TED applicable for linear modulations. The first of them is the Zero-Crossing Detector (ZCD), where the error signal is defined by the following equation:

$$e_T(n) = (\hat{c}_{n-1} - \hat{c}_n) y_R\left(nT_s - \frac{T_s}{2} + \hat{\tau}_{n-1}\right). \tag{2}$$

The second algorithm is the well-known Early-Late Detector (ELD):

$$e_T(n) = \hat{c}_n\left[y_R\left(nT_s + \frac{T_s}{2} + \hat{\tau}_n\right) - y_R\left(nT_s - \frac{T_s}{2} + \hat{\tau}_{n-1}\right)\right]. \tag{3}$$

The last one is Mueller and Mueller Detector MMD [2], which is expressed by:

$$e_T(n) = \hat{c}_{n-1} y_R(nT_s + \hat{\tau}_n) - \hat{c}_n\left[y_R(n-1)T_s + \hat{\tau}_{n-1}\right] \tag{4}$$

where $\hat{c}_n$ determines the current data estimation, $\hat{c}_{n-1}$ is the previous data estimation, y_R are filtered input sample, and $\hat{\tau}_n$ and $\hat{\tau}_{n-1}$ are estimations for current and previous samples. Note that the MMD detector operates on T_S-spaced samples, as opposed to ZCD and ELD which need $T_S/2$- spacing.

2. TED Algorithms Adjustment for DSP Implementation

Formulae (2), (3), and (4) can be applied in the DSP system immediately, but often the utilization of multiplication does not allow a high-rate of symbol transmission to be achieved [3]. The following paragraphs detail the simplification of these algorithms for PSK modulation schemes.

2.1 Modified Zero-Crossing Detector

The meaning of equation (2) is possible to be explicated as the computation of difference between inter-sample and arithmetic mean of previous and subsequent detected data. The inter-sample is defined as the level of signal sampled used exactly in the middle of the samples for data detection. In the I-Q plane we obtain two error values for the inphase component and the quadrature one. Overall error is then expressed as the sum of these components:

$$e_T(n) = e_{TI}(n) + e_{TQ}(n) = \\ = \tilde{y}_{I(n-1/2)} - \frac{\hat{c}_{I(n-1)} + \hat{c}_{I(n)}}{2} + \tilde{y}_{Q(n-1/2)} - \frac{\hat{c}_{Q(n-1)} + \hat{c}_{Q(n)}}{2} . \quad (5)$$

Considerable simplification of digital architecture can be reached by the application of low-state modulation systems (e.g. BPSK or QPSK), because the number of possible couples of detected data is limited. The arithmetic means of all combinations of previous and subsequent detected data can be saved in the memory table (bank) of coefficients. The flow diagram of this modified zero-crossing detector (MZCD) is shown in Fig. 2.

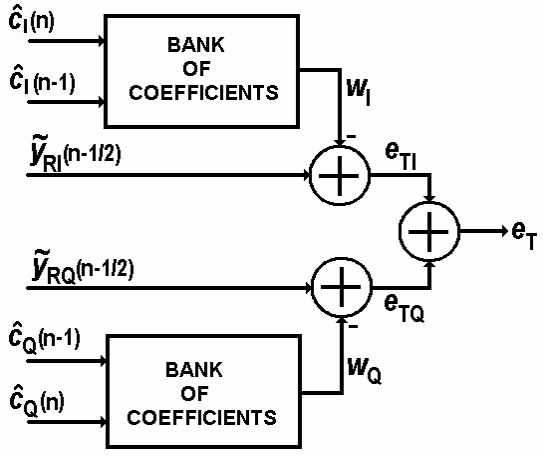

Fig. 2. Flow chart of modified zero-crossing detector.

More-state PSK modulation schemes than the QPSK requires weighting functions, which respect signal symbol distances in the inphase and quadrature axes. In these cases the timing error detector needs a multiplier or we can take advantage of fractional symbol distance ratios and apply logical shifting operations [4].

2.2 Modified Early-Late Detector

The ELD results from the symmetrical shape of the modulation pulse [5]. It performs the comparison of outrunning and delayed inter-samples. This algorithm is correct, if the previous and subsequent samples are identical, failing which an improper error determination arises. This phenomenon complicates the data detection with nonequal probabilities [6]. The insertion of a coincidence detector, which compares previous and subsequent samples, into standard ELD produces an important improvement for all types of PSK modulation schemes. The block diagram of the modified early-late detector (MELD), which is outlined in Fig. 3, indicates the operation principle. If I or Q components of previous and subsequent samples are the same, the computed timing error is enabled to the following processing. If I, respectively Q, components are unequal, the relevant timing error component is set to zero.

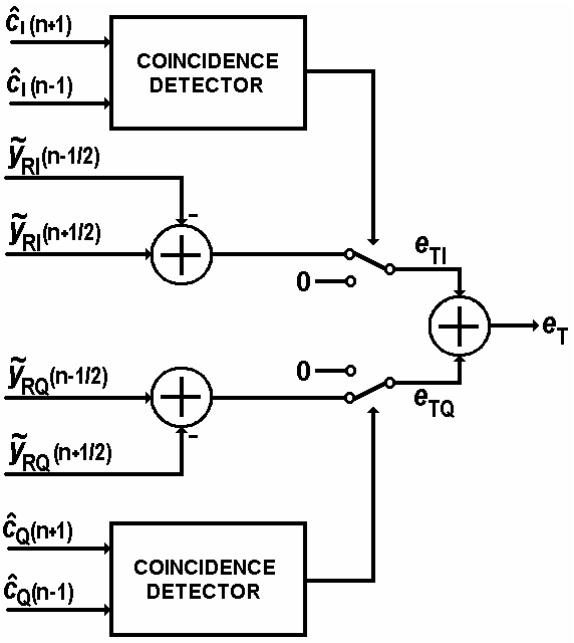

Fig. 3. Flow chart of modified early-late detector.

3. Comparison of Timing Error Detectors

The modifications in the previous chapters have been intended for obtaining more effective high-speed algorithms for digital signal processor implementation. On the other hand, some methods contribute to the improvement of detection characteristics. The variance of error quantity is the best quality index to achieving the minimal bit error ratio (BER) of the detector under test [1]. Nevertheless, the objective evaluation of detection capability requires precise definition of input signal parameters and includes: modulation scheme, characteristics of transmission channel, parameters of shaping filtration, range of normalized signal-to-noise ratio in the detector input etc., which depend on the desired application.

In the following simulations, the BPSK signals with the raised-cosine pulse shaping and additive white Gaussian noise AWGN are studied, because this configuration is the most widespread in practice. All simulations have assumed an application of the first order digital delay loop with the normalized noise bandwidth $B_{LN} = 0{,}01$. The input signal is generated by the maximum length sequence MLS with polynomial function:

$$X(D) = 1 \oplus D^6 \oplus D^7 \quad . \tag{6}$$

The MLS warrants equal data probability, which is often solved by an appropriate source encoding.

Simulations are performed for the chosen values of roll-off factor α and for the normalized signal-to-noise ratio in the range $\gamma \in \langle 0; 30 \rangle$ dB. The absolute timing error is converted into normalized delay, and is expressed by:

$$\delta_n = \frac{\hat{\tau}_n}{T_s} . \tag{7}$$

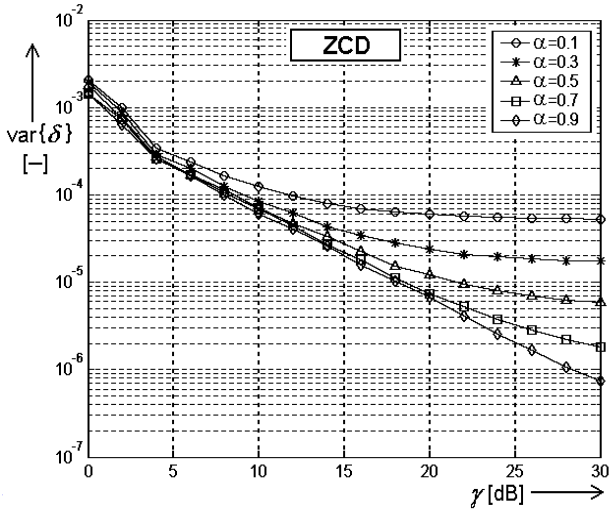

Fig. 4. Variance of normalized delay vs. normalized signal-to-noise ratio and roll-off-factor for ZCD or MZCD.

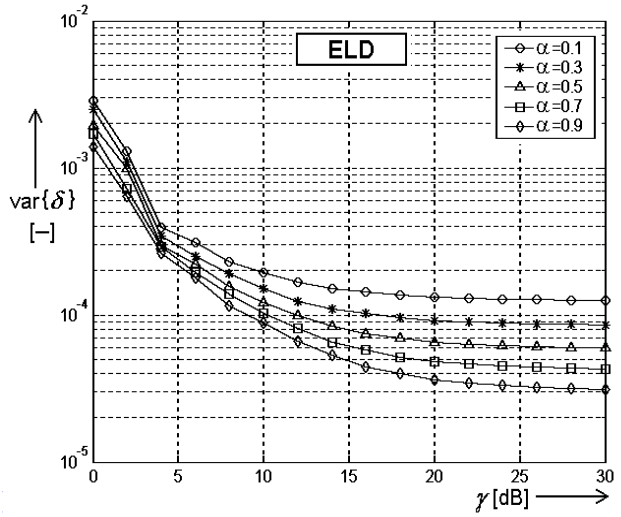

Fig. 5. Variance of normalized delay vs. normalized signal-to-noise ratio and roll-off-factor for ELD.

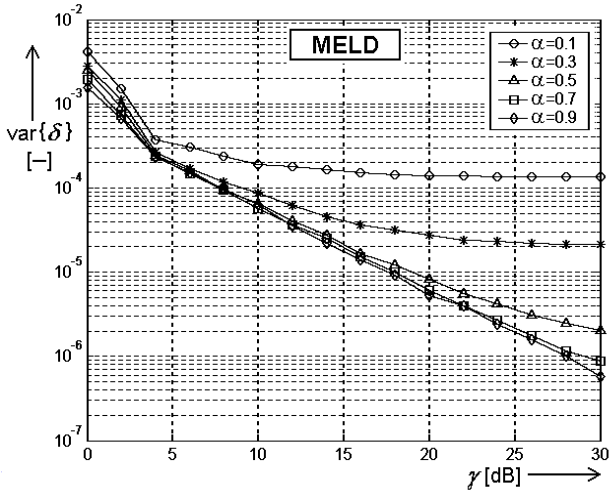

Fig. 6. Variance of normalized delay vs. normalized signal-to-noise ratio and roll-off-factor for MELD.

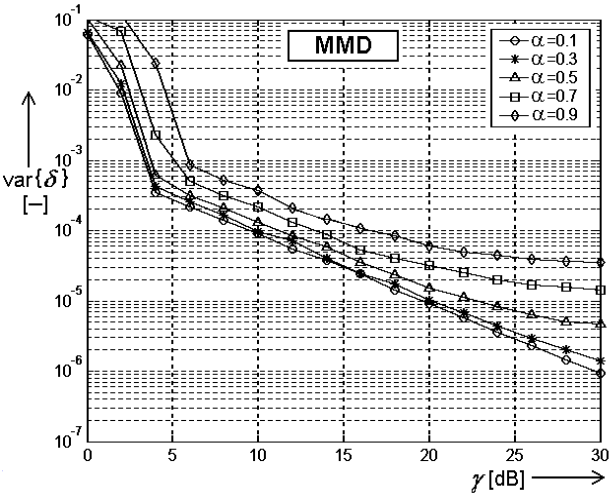

Fig. 7. Variance of normalized delay vs. normalized signal-to-noise ratio and roll-off-factor for MMD

Results of simulations are summarized in Figs 4, 5, 6 and 7, and they can be generalized for any loop parameters and equal data probability. Influence of the roll-off-factor on the variance of normalized delay is considerable and depends on the applied type of error detector. ZCD and ELD show that the variance of delay is growing for the small roll-off-factor values contrary to MMD. This effect is obvious for high values of the normalized signal-to-noise ratio. The modification of zero-crossing detector has no impact on the error variance and their characteristics are identical. The modification of early-late detector mentioned above is effective at increasing the signal-to-noise ratio with α- factor approaching one.

Simulations and their results can be useful in the selection of an optimal detector for the given application. The results from graphs 4, 5, 6 and 7 are summarized in Fig. 8, where they highlight the suitable areas (in γ-α plane) for practical applications of the described timing error detectors in BPSK demodulator.

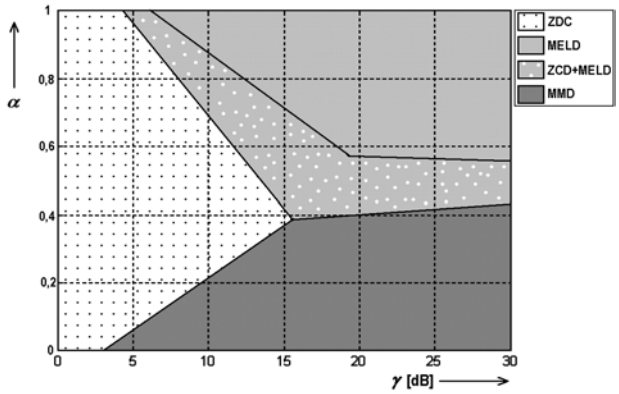

Fig. 8. The highlighted regions for optimum selection of timing error detector type in BPSK demodulator.

4. Conclusion

The application of digital systems for high symbol rate requires simplification of standard algorithms. However, this simplification cannot be the cause of decreasing characteristics from the point of view of effective signal processing. Such an approach is the subject of this paper. Two modifications of time error detector for a PSK demodulator were shown. They allow the demodulator design for high-rate data processing and reach smaller variance of delay error than the classical methods for some types of modulation schemes.

The comparison of the standard and modified algorithms for timing error detector was completed. The evaluation quantity was the variance of the normalized delay, which corresponds well with the available bit error rate. The comparison focused on the BPSK modulation scheme, but this method can be applied to any other modulation scheme.

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